filtered is easily changed in terms of design, a filtering sequence over plural channels can be changed, filtering continuity is kept, and a filtering characteristic can be changed corresponding to each channel.

【0029】

In order to achieve the above-mentioned object, a digital filter device according to the present invention comprises: one or more computing processors for generating input data strings; an input data memory for storing the input data strings; and a digital filter for reading the input data strings out of the input data memory in a predetermined order to be filtered and for generating output data strings ~~(claim 1)~~.

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【0030】

Namely, a computing (arithmetic) processor generates a plurality of input data strings. Only a single computing processor may generate these input data strings, or each of computing processors may generate one or more input data strings.

An input data memory stores the input data strings generated by the computing processor. A digital filter reads and filters the input data strings stored in the input data memory in a predetermined sequence and generates filtered output data strings.

【0031】

Thus, it becomes possible to separate an operation timing with which the computing processor generates the input data strings from an operation timing with which the digital filter filters the input data strings.

Accordingly, when the filtering by the digital filter is performed at a higher speed compared with a generation speed of the input data strings at each computing processor, it becomes possible to filter a plenty of input data strings within a single sampling period of the digital filter.

【0032】

It is also possible, for example, to sequentially filter a plurality of input data strings within a single sampling period of the digital filter, to change a filtering sequence of the input data strings, and to skip or to perform plural times filtering a certain input data string within a certain single sampling period of the digital filter.

【0033】

Also, it becomes unnecessary to strictly synchronize the operation timing of the computing processor with that of the digital filter, and it becomes easy to facilitate designing the digital filter device (timing design, circuit design, or the like), adding a computing processor, and controlling the number of input data strings (channels).

【0034】

Also, the present invention may further comprise; an output data memory for storing the output data strings generated by the digital filter, and a data processor for reading the output data strings stored in the output data memory in a predetermined order to be processed ~~(claim 2)~~.

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【0035】

Namely, an output data memory stores the output data strings generated by the digital filter. A data processor such as a DA converter reads the output data strings out of the output data memory in a predetermined sequence, to which data processing is performed.

Thus, it becomes possible to separate a timing with which the digital filter filters the input data strings from a timing with which the data processor processes the output data strings.

【0036】

Accordingly, the data processor can sequentially process a plurality of output data strings, change a processing sequence of the output data strings, and skip or perform plural times data processing of a certain output data string within a certain single period.

Also, it becomes unnecessary to strictly synchronize the timing of

the digital filter with that of the data processor, and it becomes easy to facilitate designing the digital filter device (timing design, circuit design, or the like), and controlling the number of output data strings (channels) of the data processor.

【0037】

Also, the present invention may further comprise; a switch table for associating an address of the input data memory in which the input data strings are stored with an address of the output data memory in which the output data strings are stored, and a switching controller for providing timings of reading the input data strings out of the input data memory based on the switch table and of writing the input data strings as the output data strings into the output data memory through the digital filter ~~(claim 3)~~.

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【0038】

Namely, a switch table associates an address of the input data memory in which the input data strings are stored, with an address of the output data memory in which the output data strings are stored.

A switching controller performs a switching (timing) control of reading the input data strings out of the input data memory based on the switch table and of providing the input data strings as the output data strings to the output data memory through the digital filter.

【0039】

Thus, it becomes possible to designate or change the sequence of filtering the input data strings based on the switch table.

Also, it becomes possible to switch the output data strings to a predetermined data processor corresponding to the input data strings.

【0040】

Also, the present invention may further comprise; a filter memory for storing data-under-calculation upon filtering for a first input data string before filtering for a second input data string from filtering for the first input data string, in a delay circuit included in

the digital filter, and for restoring the data-under-calculation to the delay circuit when filtering the input data string subsequent to the first input data string is started ~~(claim 4)~~. /C.D./ 11/05/2008

【0041】

The digital filter includes a delay circuit. A filter memory stores data-under-calculation, in the delay circuit, upon filtering for a first input data string before filtering for a second input data string from filtering for the first input data string.

【0042】

The filter memory restores the data-under-calculation stored when the filtering for the input data string subsequent to the first input data string is started, to the delay circuit.

Thus, it becomes possible to keep continuity of the filtered output data strings by restoring the data of the delay circuit stored in the filter memory to the delay circuit, when the digital filter, for example, shifts from a filtering state for the first input data string to a filtering state for the second input data string and to a filtering stop state for the first input data string, and then returns to the filtering state subsequent to the first input data string.

【0043】

Also, the present invention may further comprise; one or more coefficient memories for storing a filter coefficient corresponding to each input data string of the digital filter, and a filter coefficient corresponding to an input data string to be filtered may be set in the digital filter ~~(claim 5)~~. /C.D./ 11/05/2008

【0044】

Namely, a coefficient memory stores one or more filter coefficients corresponding to the input data string (channel). The filter coefficient set in the digital filter is changed to one corresponding to the input data string filtered every time the input data string changes.

【0045】

Thus, filtering corresponding to each input data string is made possible.

In order to achieve the above-mentioned object, a digital filter device according to the present invention alternatively comprises: an input data memory for storing input data strings; a digital filter for generating output data strings which are obtained by filtering the input data strings, inputted from the input data memory, and an output data memory for storing the output data strings ~~(claim 0)~~.

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【0046】

Namely, an input data memory stores a plurality of input data strings.

A digital filter generates output data strings which are obtained by filtering the input data strings in a predetermined sequence. An output data memory stores the output data strings.

Thus, it becomes possible to separate a timing with which the input data strings are written into the input data memory from a timing with which the digital filter filters the input data strings.

【0047】

Also, it becomes possible to separate a timing with which the output data strings from the digital filter are written into the output data memory from a timing with which the output data strings are read out of the output data memory.

Accordingly, it becomes unnecessary to strictly synchronize the filtering timing of the digital filter with the write timing into the input data memory, and the filtering timing of the digital filter with the read timing out of the output data memory, and it becomes easy to facilitate designing the digital filter device (timing design, circuit design, or the like), and controlling the number of output data strings (channels) of the data processor.

【0048】

Also, the present invention may further comprise; a switch table

for associating an address of the input data memory in which the input data strings are stored with an address of the output data memory in which the output data strings are stored, and a switching controller for providing timings of reading the input data strings out of the input data memory based on the switch table and of writing the input data strings as the output data strings into the output data memory through the digital filter ~~(claim 7)~~.

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【0049】

Namely, a switch table associates an address of the input data memory in which the input data strings are stored with an address of the output data memory in which the output data strings are stored.

A switching controller reads the input data strings out of the input data memory based on the switch table and provides an address storing the output data strings to the output data memory.

【0050】

Thus, the digital filter device can designate or change the sequence of filtering the input data strings based on the switch table.

Also, it becomes possible to store the output data strings which are obtained by filtering the input data strings based on the switch table in a predetermined address of the output data memory, i.e. to perform switching.

Brief Description of the Drawings

The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which the reference numerals refer to like parts throughout and in which:

Fig.1 is a block diagram showing an embodiment (1) of a digital filter device according to the present invention;

Fig.2 is a block diagram showing an embodiment (2) of a digital filter device according to the present invention;